

REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Claims 6, 9, 16, 19 and 20 were previously cancelled. Existing claims 1-5, 7, 8-15, 17, 18 and 21-24 (as previously amended) remain in the application.

ARGUMENT

Claim Rejections – 35 U.S.C. § 103

Claims 1-4, 10-14, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent 6,185,692 granted to Wolford (hereinafter Wolford) in view of US Patent 5,546,567 granted to Nakamura (hereinafter Nakamura).

Claim 1, as currently amended, is as follows (emphases added),

"a variable speed bus, the variable speed bus initialized with a first clock frequency;

a first unit coupled to the variable speed bus, the first unit having a first rate of requests to access the variable speed bus;

a second unit coupled to the variable speed bus, the second unit having a second rate of requests to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate."

Wolford does not teach or suggest at least the above emphasized portions of currently amended claim 1. Wolford does describe a data processing system including

a bus, one or more loads coupled to the bus, and a clock generator, and the clock generator dynamically sets the clock frequency for the bus in response to the number of loads coupled to the bus (see Abstract; Fig. 1; col. 3, lines 6-19, 37-42; col. 4, lines 6-12, 34-41 and 62-66 of Wolford). However, Wolford only describes change the bus clock frequency based on the number of loads coupled to the bus whether the loads are active or idle. In fact, the Examiner admitted that Wolford does not describe an arbitration and bus clock control unit that monitors the rates of requests to access the bus from various loads and determines a new clock frequency for the bus based on the rates of requests to access the bus.

However, the Examiner asserted that the feature of “change of clock frequency based on access request rate” was well known in the data processing art at the time the invention was made as evidenced by Nakamura, particularly col. 7, lines 36-41 of Nakamura. Applicant respectfully disagrees. The cited portion of Nakamura is quoted below (emphases added):

As described above, in the second embodiment, since the frequency of the operation clock of the system bus is automatically changed to a lower frequency only when *the interface having a low operation rate is accessed* while the application program is executed. Therefore, the average operation speed of the system can be maintained high.

The cited portion of Nakamura describes that the clock frequency of the system bus is reduced only *when the system bus accesses a device* that has an operation rate lower than the clock frequency of the system bus. Further support for this statement can be found at col. 6, lines 35-51 of Nakamura, which is quoted below (emphases added):

.... Assume that a CPU 11 transfers data to an external device 34 via an interface 32 which can be operated only at a low clock frequency while the application program is executed. When the CPU 11 executed an output command in the application program for the interface 32, the CPU 11 generates and supplies an output instruction to a Direct Memory Access Controller (DMAC) 30 according to a basis input/output system program stored in the BIOS ROM 20. The DMAC 30 reads out data from a memory section 17 in response to the output instruction and transfers the read-out data to the external device 34 via the interface 32. When all the data is completely transferred, the DMAC 30 generates a completion notice to the CPU 11. A bus controller 22' monitors the output instruction from the CPU 11 to the DMAC 30 and the completion notice from the DMAC 30 to the CPU 11, and programmatically sets the operation clock frequency of the system bus from 10 MHz to 8 MHz. ...

In marked contrast, claim 1 recites "an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate" (emphases added). In other words, what is monitored is the rate of requests from a device coupled to a bus, but not the operation rate of the device itself as disclosed in Nakamura. Such a difference is not trivial because a device's access request rate to a bus and the device's own operation rate are two different things and they are not equivalent. Nakamura does not disclose the feature of changing clock frequency of a bus based on access request rates by devices coupled to the bus.

The Examiner also asserted that the claimed limitation is straightforward possibility in the art and does not require the exercise of inventive skill. Applicant also disagrees. Changing of a processor's clock frequency is known for a while as showing by different power saving states. For example, when there is no activity including memory access activity, the processor may be put in "hibernation" or "standby" state,

which basically changes the clock frequency of the processor. For so many years when the technology for changing a processor's clock frequency is known, no one (at least none has been found yet) has ever come up with a technology for changing the clock frequency of a bus until the disclosed application. Indeed, the present application discloses a technology that solves a long-felt problem and is more effective than changing the clock frequency of the entire processor to conserve power consumption of a computer. Thus, the claimed limitation is not obvious over Wolford in view of Nakamura. Applicant respectfully requests that the 35 U.S.C. 103 rejections of claim 1 be withdrawn.

Independent claim 10 includes similar limitations to those emphasized for claim 1 above. Based on the arguments presented above for claim 1, claim 10 is not obvious over Wolford in view of Nakamura. Because independent claims 1 and 10 (as amended) are now patentable over Wolford in view of Nakamura, all of the claims that depend therefrom (i.e., claims 2-4, 21 and claims 11-14; respectively) are also patentable over Wolford in view of Nakamura. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections of claims 1-4, 10-14, and 21 over the combination of Wolford and Nakamura be withdrawn.

Claims 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wolford in view of Nakamura, and further in view of Barr.

As mentioned above, the combination of Wolford and Nakamura does not teach or suggest all of the limitations recited in independent claims 1 and 10. Barr was not cited to cure those deficiencies in Wolford or Atkinson. Because claims 22-23 depend

from independent claim 1 and claim 24 depends from independent claim 10 and because independent claims 1 and 10 are patentable over Wolford in view of Nakamura, and further in view of Barr, claims 22-24 are thus patentable over Wolford in view of Nakamura, and further in view of Barr. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections over Wolford in view of Nakamura and further in view of Barr of these claims be withdrawn.

Claims 5, 7, 8, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolford in view of Nakamura, and further in view of common knowledge in the data processing art at the time of the invention.

As mentioned above, the combination of Wolford and Nakamura does not teach or suggest all of the limitations recited in currently amended independent claims 1 and 10. The common knowledge in the data processing art was not cited to cure those deficiencies in Wolford or Nakamura. Because claims 5, 7, 8 depends from independent claim 1 and claims 15, 17, and 18 depends from independent claim 10 and because independent claims 1 and 10 are patentable over Wolford in view of Nakamura, and further in view of common knowledge in the data processing art, claims 5, 7, 8, 15, 17 and 18 are thus patentable over Wolford in view of Nakamura, and further in view of common knowledge in the data processing art. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections over Wolford in view of Nakamura and further in view of common knowledge in the data processing art of these claims be withdrawn.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in condition for allowance, and their passage to issuance is respectfully solicited. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

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